On Applying Non-Classical Defect Models to Automated Diagnosis

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Abstract

Automated fault diagnosis based on the stuck-at fault model is not always effective. This paper presents practical experiences in applying a bridging fault based diagnosis technique to a TI ASIC design. Results are presented for units into which known bridging defects have been introduced via a focused ion beam (FIB) machine.

1 Introduction

Integrated circuit (IC) technologies have reached the stage where the inclusion of more than one billion transistors on a monolithic piece of silicon is not only possible but likely in the near future. Such extremely high levels of integration complicate the entire IC manufacturing process. Several crucial test-related steps that are affected are initial system debug, the ramp to volume production, the yield improvement phase, and volume manufacturing testing itself. In all of these manufacturing phases, the higher the level of integration, the more complicated the task. Increased competition in the IC marketplace demands that all of the aforementioned manufacturing steps be executed as quickly as possible, with time frames that may range from a few days to a few weeks at the very most. Without powerful system debugging aids, such goals are impossible to meet.

A key tool that aids in all these areas is automated diagnosis. Since there are numerous potential sources of errors for highly integrated silicon products, and visual debugging is often ineffective, the IC manufacturing industry is becoming increasingly dependent on these tools.

In the most commonly used scenario, a large IC is designed with full scan (or something approximating it). The scan patterns that are applied to the device not only provide a rigorous manufacturing test, but they also can provide a wealth of debugging information. The problem then becomes how to analyze the data.

Most commercial automated diagnosis tools rely on the stuck-at fault model [1] as a basis for these analyses. However, it has been shown repeatedly that the stuck-at fault model does not accurately reflect the behavior of current generation silicon defects [2]–[11]. While it is desirable to move to a more realistic model of silicon behavior, it is not desirable to give up the performance of commercial tools based on classical fault models, nor to dramatically change the design flows used to generate the initial test patterns.

This paper describes a technique that uses stuck-at fault-based information to more effectively diagnose defective chips that are difficult to diagnose any other way. Section 2 presents the motivation for the proposed technique in more detail. Section 3 discusses FA flows that are based on test results. Section 4 gives a brief overview of the philosophy behind the new diagnosis technique. Section 5 reviews the design-for-testability features of the device used in this experiment. Section 6 details some of the pitfalls to the application of the methodology, along with suggested solutions and workarounds. Sections 7 and 8 describe FIB techniques and selection of FIB sites. Finally, the results of an experiment in which artificially induced defects are placed in working devices are described in Section 9, followed by conclusions and suggestions for further study.

2 Motivation

Failure analysis tool developers have provided many different tools and techniques for the localization of defects on large silicon devices. Examples of these tools include optical microscopy, liquid crystal techniques, emission microscopy, electron beam probing, resistive contrast imaging [12], CIVA [13], LIVA [14], and LECIVA [15]. However, improving IC manufacturing technology continues to present challenges. In a highly competitive manufacturing situ-

ation, there simply may not be enough time to rely solely on physical analysis due to the highly intricate and time-consuming nature of the work.

The IC industry is responding to this challenge with test-based automated diagnosis. Traditional stuck-at fault based diagnosis techniques have been around for some time [16], [17]. More recent innovations have included quasi-bridging fault techniques [9], [18] and diagnosis based on responses to I_{DDQ} testing [19]–[23].

Diagnosis based on single stuck-at fault modeling is valid in many situations and has been successfully applied by the authors to multiple devices [24]–[27]. However, experience and experimental evidence suggests that in certain situations, the single stuck-at fault model may yield poor diagnoses or no diagnoses at all [27]. In such cases, it may be desirable to retry diagnosis with alternative methods before destructive physical analysis is employed.

I_{DDQ}-based diagnosis has proven to be relatively simple to apply and reasonably accurate [20]–[23]. However, if a defect does not induce detectably abnormal currents, it may not lead to a diagnosis. Furthermore, depending on the capabilities of the equipment in the failure analysis area, one may not be able to effectively measure I_{DDQ}.

For these reasons, and because bridging faults are believed to be a common defect type [6], [7], the authors have chosen to pursue the application of bridging fault diagnosis in manufacturing diagnosis and debug situations. However, few commercial tools are available that support bridging fault extraction and simulation, especially for very large circuits. It is therefore desirable to make use of existing single stuck-at fault simulation information in order to achieve bridging fault diagnosis. Techniques first proposed by Millman et al. [9] and made workable by Chess et al. [18] are ideally suited for this purpose. An application of a similar technique to the UltraSPARC^{TM}-I processor has been presented in [28].

However, there are a number of practical issues that must be addressed in order to successfully use these new bridging fault modeling and diagnosis techniques. How will the fault dictionary be created? Is it possible to generate the proper fault dictionary format from the fault simulation output of a commercial tool? These issues and more are discussed in this paper.

Besides the aforementioned problems, there are also issues relating to the extraction of the bridging faults themselves. Often, in a multi-vendor tool environment, it may be difficult to relate schematic and netlist information to one another, thus making the extraction of realistic bridging faults difficult. The protection of intellectual property is also important, and a detailed list of extracted adjacent signal lines may compromise it. Therefore, it is desirable to develop diagnosis techniques that do not require the use of physical design information. That problem was addressed in a preceding paper [29]. The techniques reported there are utilized in this study.

Finally, there are numerous studies indicating the limitations of tests generated using the stuck-at fault model for detection of actual defects, particularly in MOS technologies, including those cited above plus others [30]–[33]. It is therefore a natural extension to question the efficacy of the same tests for purposes of diagnosis. The results reported here indicate that there may be limitations to the accuracy of diagnosis achievable when relying on stuck-at-based test sets for defect diagnosis.

3 Test-Based FA Flow

There exists an array of powerful IC physical failure analysis tools, but increasingly complex fabrication techniques are posing threats to their continued viability. Test-based diagnostic techniques hold promise for providing guiding information to the failure analyst as to where and how to apply physical analysis tools.

There are a number of test-based diagnostic techniques that will result in varying degrees of successful isolation based on the defect instance, the fault model used, and other parameters. How the various techniques are employed and in what order is an important question to address.

A simple failure analysis process flow has been proposed in an earlier publication [27], but it should be augmented to reflect the existence of multiple test-based diagnostic tools. One possible scenario is diagrammed in Figure 1.

The analyst might wish to precede the test-based diagnostic analyses with simple analytical tools such as visual inspection or perhaps liquid crystal techniques. If those techniques do not yield satisfactory results, then test-based techniques might be applied. At each decision point in the test-based flow, the analyst must decide if:

- The device to be analyzed failed the relevant test, and
- The corresponding tools are available to the analyst.

If those criteria are met, then the flow in Figure 1 might be implemented. I_{DDQ} is chosen as the first

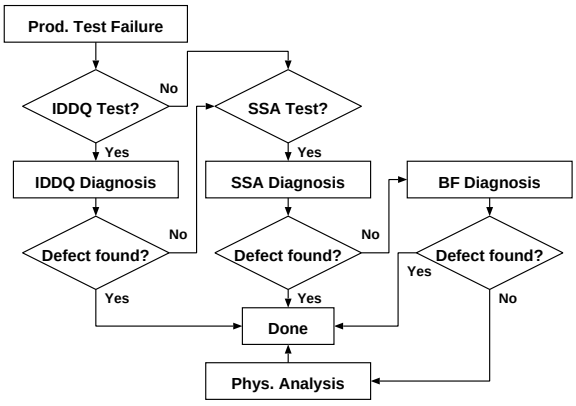

Figure 1: A diagram showing the flow through various test-based diagnostic procedures

test-based technique due to its relative simplicity, that is, I_{DDQ} diagnosis requires only failed pattern information, as opposed to failing patterns *and* observation sites that may be required in single stuck-at test-based diagnosis. Stuck-at test-based diagnosis is in general simpler to use than the composite signature bridging fault diagnosis discussed in this paper.

An alternative approach is one presented in a companion paper [34]. That approach is built around a probabilistic evaluation of a set of fault candidates given all the available data about a failing circuit. The introduction of probability as a common measure of diagnostic inference allows different algorithms to process different sets of data, using different sets and types of candidates, to produce a single diagnostic result. The current system works with just two models: bridging faults and single stuck-at faults. The diagnostic bottom line will be: if the behavior looks most like a bridging candidate, score the bridge highest; if it looks most like a stuck-at candidate, score the stuck-at candidate highest; if neither happens, give some indication that the behavior is not much like any of the candidates, bridging or stuck-at. In the first case, the defect will be assumed to be a signal-line short; in the second, the identification will be less precise—the defect could be any of several that behave like a stuck-at fault; in the third case, the diagnosis is unsuccessful. Further development of this system will be required before it can completely replace the multi-tool flow presented in Figure 1. Results of using this implementation are presented later in this paper.

If the application of a test-based diagnostic technique results in one or more candidate defect sites being indicated, then one must carefully apply non-destructive physical analysis technique to determine if a defect has indeed been found. Only if the presence of a defect has been confirmed would the analyst then use destructive techniques for further defect characterization. Also, if all test-based techniques are exhausted and no defect is found, the analyst must resort to physical techniques, possibly destructive, to attempt to locate the anomaly.

4 The UCSC Diagnosis Approach

Most, if not all, diagnostic techniques assume some mechanism of failure. Many use a single fault model and assume the defect is a-priori an instance of that model. Others, supposedly more general, assume the source of the failure to be either a single circuit node or some additive combination of single-site failures. The fact is, however, that it is generally not known ahead of time what sort of defect is present or which fault model best represents the failure. Even if the fault model is chosen perfectly (that is, the actual defect is one targeted by the chosen model), there is no guarantee that the defect will behave as modeled. In fact, there is considerable evidence suggesting that unmodeled behavior is the norm, and not the exception, in modern VLSI circuits [35].

The UCSC approach allows the application of multiple fault models with the ability to evaluate which model and which instance seems best for the faulty behavior seen. The UCSC approach uses a probabilistic approach because of its important advantages:

1. Because faults are ranked according to their estimated probability of occurrence, the system can provide diagnoses that compare faults from different models in the same diagnosis [34].

2. The system can tolerate imperfect fault modeling and noisy data [11].

3. The system can make use of information from disjoint sources including inductive fault analysis, structural path tracing, logical failure diagnosis, quiescent current diagnosis, and probabilistic physical failure analysis [34].

The current implementation provides diagnoses that rank stuck-at and bridging faults using only logical failure information. Predictions about the behavior of bridging fault candidates are derived in an inexpensive manner from stuck-at fault signatures [18].

The next section discusses briefly the design for testability features of the circuit used in the study. Section 6 presents the problems we encountered when applying the UCSC technique to this and other designs.

5 Device Description, DFT and Test Features

The device used in this study is a data buffering chip. It's function is to connect a microprocessor and its E-cache to a data bus. It was designed as an 80K gate array, using Texas Instruments' TGC3000 ASIC library. The library is characterized by a physical gate length of .6μ, and L_{eff} of .52μ. The device operates at 3.3V and at speeds ranging from 75-100 MHz. It is packaged in a multi-power-plane ball grid array package.

For testability purposes, both JTAG boundary scan and full internal scan are implemented. Internal scan operations are controlled by the JTAG TAP and utilize the TAP pins for scan access. There is one scan chain consisting of 2881 scannable D-type flip-flops (FFs). Even though scan patterns from another tool were already available, scan patterns were generated using Mentor Graphics' FastScan^{TM} automatic test pattern generation (ATPG) tool. This was done so that FastScan^{TM}'s stuck-at diagnosis function could be compared with bridging fault diagnosis. A very high stuck-at fault coverage was achieved with 792 uncompressed scan patterns.

6 Practical Considerations

This section discusses some of the practical limitations that were overcome when the UCSC technique was used on the data buffer chip and several other large designs.

To use this technique effectively, the following information is required:

- Netlist, test patterns, and layout.
- Stuck-at dictionary for all faults.
- Realistic bridging fault set.

Not all of this data was made available to the team at UCSC due to the necessity to protect proprietary data.

6.1 Netlist, Test Patterns, and Layout

The situation of not having access to the netlist and layout had the following implications:

- Match restriction [18] could not be performed completely. Simulation of test patterns was not possible to determine if opposite or similar values were placed on bridged nodes. This information could have been extracted from an I_{DDQ} bridging fault dictionary if one had been available.
- A limited form of match restriction was performed. If stuck-at faults of the same type were detected by a pattern on both the nodes being considered, then that pattern was dropped before performing the matching. This information was available in the fault dictionary.
- No layout information could be made available, so extraction of realistic bridging faults using CARAFE was not an option.

6.2 Stuck-at Fault Dictionary

To create the stuck-at fault dictionary in the format used by the UCSC software [36], the test patterns were simulated in Mentor Graphics' FastScan^{TM} to provide failing pattern information for each stuck-at fault, and the resulting information was converted to the UCSC format. The fault dictionary is in an encoded form, which does not contain fault names, test patterns, or scan cell names.

The complete fault dictionary was not used in the diagnosis. The number of faults used was in the range of about 20,000 faults, which represents all detected stuck-at faults on all gate outputs after fault collapsing was performed.

6.3 Realistic Candidate Bridging Fault List

Due to the absence of layout information, we adopted the methodology documented in our previous publication [29], which describes two different approaches.

The first is to use traditional stuck-at diagnosis to identify at least one node in the bridge. Having done this, the highly-ranked nodes from the stuck-at fault diagnosis are paired with each node in the stuck-at dictionary to create a candidate bridging fault list.

The second approach (not employed here) involves constructing a node signature that is the union of the stuck-at-0 and stuck-at-1 signatures for a node. The number of node signatures is n for an n-node circuit, while the number of composite entries is $\binom{n}{2}$. The diagnosis now involves performing a match based on node signatures and pairing every resulting top-ranked candidate with other nodes in the circuit to generate a candidate list.

7 Focused Ion Beam Techniques

A number of working chips were obtained, and defects were introduced using a focused ion beam (FIB) machine. To utilize a FIB device to bridge two signal lines, e. g., two METAL 2 lines, a hole is drilled through the oxide layers until the metal layers are exposed. Platinum material is then deposited in the

holes to make contact. The contacts are then bridged using a strap of platinum material creating a bridging defect. Xenon diflouride (XeF_2) gas is used to accelerate the oxide etch to create the contact hole. The XeF_2 gas also reduces redeposition of sputtered material and etches a contact hole with steeper sidewalls. The platinum is deposited via a gas with a hydrocarbon carrier. The resistance of the contact material is usually on the order of 150-200 Ohms/μ^2 while that of the metal strap is 20 Ohms/μ^2. Neither of these resistances is as good as pure platinum due to the impurities introduced by the carrier gas. Typical FIB deposited metal can contain up to 30% carbon. Though the same material is used for both the contact and the strap, the contact resistance is higher due to the fact that more of the carrier gas gets trapped along with the platinum inside the FIB hole and some voiding can occur during deposition.

8 Defect Site Selection

Detailed FIB data is given in Table 1. In the first two trials, characterized here by FIBx and FIBy, the failure analyst selected sites at which to instantiate FIBs based only on convenience and adjacency of nets. Analysis of some of those initial results, detailed in Section 9, led the authors to a more systematic way of selecting FIB sites.

First, it was decided to compare the effects of two types of bridging faults (as always, bridges between gate outputs): *intra-gate* and *inter-gate* bridges. An intra-gate bridge is a bridge between two outputs that feed the same gate, and an inter-gate bridge is a bridge between two outputs feeding different gates. In each FIB instance for FIBs 1-6, three individual sites were selected, generically referred to as A, B, and C in Table 1. In each case, sites A and B feed the same gate, and site C feeds a different gate. FIBs are labeled with the subscript *intra* or *inter* to indicate they are either an intra-gate or inter-gate bridging defect, respectively. FIBs 7-9 were not subject to the *inter* and *intra* gate criterion.

Another parameter being investigated is the role the number of detections plays in the diagnosability of the defect. In order to study this phenomenon, it was necessary to rank all the faults in the fault dictionary according to their detections. We calculated the detections as the total number of simulated failing bits for the stuck-at-0 and stuck-at-1 faults on the sites for the test pattern set used on this device. So, for example, if a fault fails a total of two patterns, the first with three scan FFs failing, and the second with 10 scan FFs failing, then the detections measure for this fault is 13.

Using this scale, the range of detections is anywhere from 1 to 2,281,752—the latter being the product of the number of scan FFs and the number of scan patterns. We wanted to choose FIB sites across this spectrum, to get a representative set of FIBs with various detectabilities. No detectability analysis was performed prior to the selection of FIBx and FIBy, hence the blank entries in the second column of Table 1.

It was therefore desirable to satisfy a number of criteria when selecting the sites at which to FIB bridging defects, but the overriding constraint was always the layout of the device and the adjacency of various sites. All of the experimental criteria were satisfied to the degree possible given that primary limitation.

As a control for the experiment, and to checkout all tools in the study, we inserted stuck-at defects into two devices. The node selected was the C node of $FIB6_{inter}$, and both stuck-at-1 and stuck-at-0 were inserted, one each in the two devices.

9 Results and Analysis

In this section, we present the results of various diagnosis trials on the FIBs in Table 1 above. The diagnoses are also analyzed for any interesting results that are evident.

9.1 Correlation Between Tester Fails and Simulated Fails

For each of the bridges FIBbed, the corresponding bridging fault was injected by modifying the netlist. All the scan patterns were then re-simulated on this netlist under the assumptions of wired-AND, wired-OR and wired-X. Under the wired-X assumption, the output of the bridge is an `X` if the two bridged nodes are driven by opposite values. These simulations produce information on failing bits and failing patterns under the three different assumptions. For the wired-X case, the fault is considered possibly detected if the output in the good circuit is `0` or `1` and in the faulty circuit is `X`. Column 3 of Table 1 shows the number of failed bits in simulation under the three different assumptions for all FIBs. Note that this simulation does not take into account the Byzantine General's problem for bridging faults. All simulations were done using Mentor Graphics FastScan^{TM}.

Column 4 of Table 1 shows the number of bit fails on the tester for each of these bridges FIBbed. In many cases, there is a very strong correlation between tester fails and a wired-AND simulation. This is evident in $FIB3_{inter}$, $FIB4_{intra}$, $FIB4_{inter}$, $FIB5_{intra}$, $FIB6_{intra}$ and $FIB6_{inter}$. In fact, all but two of these were exact matches with the wired-AND simulation.

Identifier	S-0/S-1 sim. bit fails	AND/OR/Wire sim. bit fails	tester bit fails
FIBx		277/259/536	131
FIBy		4/4/4	4
$FIB1_{intra}$	A: 2442/36 B: 2442/25	0/61/66	28
$FIB2_{intra}$	A: 25913/2731 B: 4069/1303	8374/2888/11262	992
$FIB3_{inter}$	A: 51525/5994 C: 54350/7839	50706/53189/58823	50625
$FIB4_{intra}$	A: 15/2 B: 18/2	33/0/33	33
$FIB4_{inter}$	B: 18/2 C: 24/13	8/12/20	8
$FIB5_{intra}$	A: 13150/21221 B: 7555/176	181/21359/22674	180
$FIB5_{inter}$	A: 13150/21221 C: 21230/12662	20297/22374/42572	7943
$FIB6_{intra}$	A: 100/278 B: 190/202	212/242/410	212
$FIB6_{inter}$	A: 100/278 C: 505/49	121/230/351	121
FIB7	A: 2477/141 B: 2477/45	-	2477
FIB8	A: 6738/7520 B: 6515/7560	7066/7046/14112	3467
FIB9	A: 58/164 B: 188/505	340/130/470	252

Table 1: A table describing simulated and actual tester failure data for FIBbed defects.

$FIB3_{inter}$ behaved very much like a wired-AND except that the last pattern failed in simulation on 81 bits, but not on the tester. For $FIB5_{intra}$, the simulation and actual fails differed only by one bit. $FIB2_{intra}$ and FIBx exhibited tester fails that were a subset of the wired-OR simulation. FIB8 behavior was a subset of wired-AND simulation and FIB9 behavior was a superset of wired-OR simulation. FIBy had the same results for wired-AND, wired-OR and wired-X simulations. The reason for this is explained in Section 9.3. FIB7 was a feedback bridge that was not simulated.

9.2 Diagnosis Results

The results of the various diagnosis trials are summarized in Table 2. The FIB identifiers and the tester bit fails (column labeled "tester") are the same as those in Table 1. FastScan^{TM} results are reported in the third column. They are of course based on stuck-at diagnosis, and the possible outcomes are none, one, or both of the two nodes in the bridge appearing in the diagnosed candidate list.

The results from the UCSC diagnosis tool are reported in the last column. The tool was run in a mode which combines stuck-at and bridging diagnosis using probabilistic techniques as discussed in Section 4. The tool was limited to output no more than 10 diagnosed candidates. The possible outcomes are:

- A bridging candidate containing both nodes in the actual bridge.
- A bridging candidate containing one node in the actual bridge.
- Both bridged nodes appearing as stuck-at candidates.
- One node appearing as a stuck-at candidate.
- Neither node appears as either a stuck-at or bridging candidate.

The two control stuck-at FIBs were both diagnosed correctly by both tools as stuck-at faults. This result provided more confidence in the subsequent results for the bridging FIBs.

Identifier	tester	S-a diag	Mixed diag
FIBx	131	one node	one node s-a
FIBy	4	none	one node bridge
$FIB1_{intra}$	28	one node	two nodes bridge
$FIB2_{intra}$	992	none	none
$FIB3_{inter}$	50625	one node	two nodes bridge
$FIB4_{intra}$	33	none	two nodes bridge
$FIB4_{inter}$	8	one node	one node bridge
$FIB5_{intra}$	180	one node	two nodes bridge
$FIB5_{inter}$	7943	one node	two nodes bridge
$FIB6_{intra}$	212	one node	two nodes bridge
$FIB6_{inter}$	121	two nodes	two nodes bridge
FIB7	2477	two nodes	one node bridge
FIB8	3467	one node	one node bridge
FIB9	252	one node	two nodes bridge

Table 2: A table describing diagnosis results for two different tools.

9.3 Analysis

The results in Table 2, while "close" in many instances, still did not always result in accurate bridging fault diagnosis. One might be tempted to conclude that there are deficiencies in the modeling used or the algorithms employed. However, careful analysis of samples of the data show that other factors are at work, as is detailed below.

FIBx: A portion of the layout indicating the location of this FIB is shown in Figure 2. The corresponding photographic image of the FIB is shown in Figure 3.

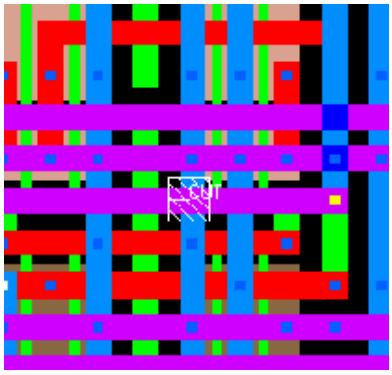

Figure 2: A portion of the layout showing the location of FIBx.

Diagnosis on this FIB yields several bridging fault candidates. One of these candidates is one of the two nodes in the actual FIB. Errors on the tester are observed in the FF in the forward cone of logic of this bridged node. The other bridged node does not have any effect on the observed response.

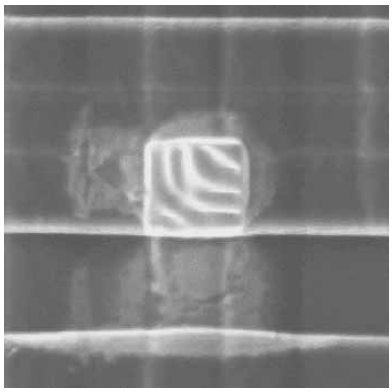

Figure 3: A photographic image of FIBx.

The defect instantiation is shown in Figure 4. The bridge occurs at node A and B, outputs to buffers that feed FFs after passing through two-input multiplexors.

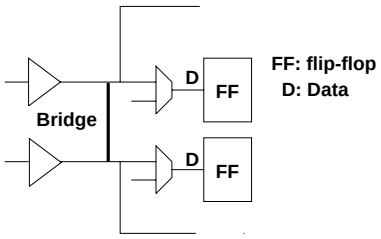

Figure 4: A diagram showing the logic around FIBx.

Both `01` and `10` values appeared on the two nodes, A and B, as verified by simulation. The behavior therefore does not mimic wired-AND or wired-OR. The FIB behaved like a pseudo-wired-OR, where one node dominates the other. Thus a `1` on A and `0` on B forces A to a `0`; but a `0` on A and `1` on B does not cause any error. The errors exhibited are therefore a subset of the errors that would have been caused had a stuck-at fault been present on the dominant node.

FIBy: This FIB bridges the two inputs within an XOR tree. This results in the wired-OR, wired-AND and wired-X simulations to yield the same result. In this case, the bridging fault behaves exactly like the output of the XOR tree stuck-at-0. The result of this experiment motivated the intra-gate and inter-gate criteria used for FIB site selection described in Section 8. We wanted to determine

if majority of intra-gate bridges tend to be diagnosed as a stuck-at fault. The results however indicate that this may not necessarily be so.

FIB4$_{inter}$: Only one node was present in a bridging candidate resulting from this diagnosis. Tester fails are observed in the cone of logic of one of the bridged nodes only. In this case, the tester failures are exactly similar to wired-AND. However, on simulating the pattern set, it is seen that only a `10` pattern appeared on the bridged nodes, so only the first node sees errors. The second node is never erroneous and thus does not show up in the diagnosis at all. This unit demonstrates the need for careful selection of the pattern set, e. g., via some form of diagnostic ATPG. Even though the stuck-at test set detects this bridging fault, as both `10` and `01` patterns do not appear on the two nodes, diagnosis does not identify the bridge.

FIB5$_{intra}$: The bridge is present in the diagnosis, but is the 8th candidate. In this case also, the fault effect is present in the forward cone of logic of only one of the nodes. The fact that the second node shows up in the diagnosis is fortuitous. In this case, however, both `10` and `01` patterns appear on the bridged nodes. Figure 5 shows a logic diagram near the FIB.

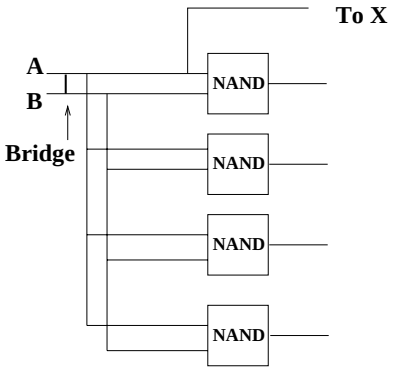

Figure 5: A diagram showing the logic around FIB5$_{intra}$.

The two nodes A and B of the bridge are inputs of NAND gates. In addition A fans out to another gate X that B does not affect. As this FIB behaves like a wired-AND, the fault effect is blocked from being propagated at the NAND gates. This bridging fault is therefore observable only via X. In this case, even though both `01` and `10` patterns appear on nodes A and B, the wired-AND behavior at the inputs of the NAND gate causes fault blocking.

FIB7: This bridge is a feedback bridge as depicted in Figure 6.

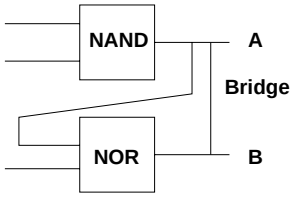

Figure 6: A diagram showing the logic around FIB7.

This is an interesting case because the stuck-at diagnosis produces both nodes. When B shows up in the diagnosis, so does the input to the NOR gate that is fed by A due to fault equivalency relationships.

10 Conclusions

We have explored the application of non-traditional fault diagnosis techniques to practical design situations with actual semiconductor devices. A comparison has been performed between traditional stuck-at based diagnostic techniques and bridging fault-based diagnosis. Defects with varying numbers of detections for a particular test pattern set were examined, and the effects of intra-gate and inter-gate bridges were compared.

Even though the bridging fault diagnosis tool seems well-matched to the FIBbed bridges in this study, it still has the drawback of having no access to physical information (e. g., the netlist) when compared with FastScan^{TM}, which performs diagnostic fault simulation on the actual design. One might therefore have reasonably expected that the bridging fault diagnosis results would suffer due to that limitation. However, in spite of the lack of physical information, bridging fault diagnosis worked quite well in many instances.

We were surprised to note several instances of near ideal wired-AND behavior. How the errors are observed (how the defect is made manifest) may be influenced by test data applied. In more general terms, the content of the test data may validate or invalidate any of the possible models used to diagnose.

We also encountered three cases where the bridging fault was acting in in a 'unidirectional' manner. In FIB8, FIBx and FIB2$_{intra}$, the failing patterns were a subset of either wired-AND or wired-OR behavior. On examining these further, it seemed that one node was always dominating the other. We conjecture that this may be due to differences in resistances when

traversing across different layers of metals in interlayer shorts.

In another case, perfect stuck-at behavior was manifested by a bridging fault not involving a power rail. This is probably not unprecedented, but does point out yet again the utility of stuck-at based diagnosis in some situations.

Though not reported in Table 2, the authors also compared the accuracy of pass/fail and output measure diagnoses. Pass/fail diagnosis uses only the failing pattern numbers to distinguish among candidates, while output measure diagnosis utilizes failing pattern numbers as well as the observation points (scan FFs and/or output pins). The results of this study seem to indicate that output measure diagnosis is required to ensure reliable results, which contradicts earlier studies done by the authors on other FIBbed devices.

The two parameters studied, detectability and intra-gate versus inter-gate effects, seemed to have no influence on the accuracy of the diagnoses. However, before any conclusions can be drawn, more data is required.

In summary, there appears to be no one diagnosis technique that will always result in accurate results for any situation. Any given defect may validate or invalidate any of the known diagnosis fault models. One example is the unidirectional wired AND and wired OR behavior that is not explained by a conventional bridging fault model. Continued refinement of fault models is needed, or perhaps a more fault-independent approach is warranted.

11 Future Work

The authors intend to apply these techniques to actual failed devices. Finally, recent work has defined the notion of Excitation Bias or E-Bias in ATPG [33]. E-Bias essentially means that the manner and frequency of defect detections is greatly influenced by the fault model used by the ATPG tool to generate the test set. So, for example, a test set generated for rapid detection of single stuck-at faults, while capable of detecting actual bridging defects, may not suffice to accurately *diagnose* them. In some sense, the fact that a particular test set used for diagnosis purposes may only excite a defect in a limited way is related to the E-Bias of the test set with respect to the defect. If a test set could be created with minimized E-Bias with respect to all defects, the authors conjecture that that test set would have enhanced diagnostic properties when compared to conventional ATPG tests. The authors would like to investigate that phenomenon and report it in a future publication.

12 References

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